REMARKS

Claims 1 - 22 are pending, of which claims 17 - 20 have been withdrawn from consideration. By this Amendment, claims 1, 2, 14 and 21 have been amended, and new claim 22 has been added. The applicants respectfully submit that no new matter has been added. It is believed that this Response is fully responsive to the Office Action dated February 23, 2001.

Examiner Telephone Interview:

The courtesy extended by Examiner Chen during the June 22, 2001 telephone interview is gratefully acknowledged. The substance of discussions during the interview are incorporated into the following remarks.

As to the Merits:

As to the merits of this case, the Examiner maintains the following rejections:

(1) claims 1 - 16 stand rejected under 35 U.S.C. 103(a) as being anticipated by **Mochizuki et al.** (of record) in view of **Ochiai** (of record) or **Watanabe et al.** (of record); and

(2) claims 1 - 13 and 16 stands rejected under 35 U.S.C. 103(a) as being unpatentable over **Ochiai** or **Watanabe et al.** taken with **Zafar** in view of **Kawai et al.** (of record) **Yamazaki et al.** (or record).

Both of these rejections are respectfully traversed.

Significant structural arrangements of the applicants' claimed invention, as amended, now includes forming a local interconnection covering an entire portion of the upper electrode with an area which is larger than an area where the upper electrode contacts with the oxide dielectric film in a plan view, in a range which passes through the first opening and the second opening, by patterning the metal film; and forming a third insulating film for covering the local interconnection.

None of the applied references, singly or in combination, teach or fairly suggest the significant structural arrangements of the applicants' claim invention concerning forming a local interconnection covering an entire portion of the upper electrode with an area which is larger than an area where the upper electrode contacts with the oxide dielectric film in a plan view, in a range which passes through the first opening and the second opening, by patterning the metal film; and forming a third insulating film for covering the local interconnection.

It is a purpose of the invention to prevent deterioration of polarization-characterization caused by a diffusion of hydrogen in the step of forming the third insulating film and the local interconnection by a CVD using a reduction reaction. Therefore, the local interconnection is formed on the capacitor as covering an entire section of the upper electrode of the capacitor, and the local interconnection becomes the layer for preventing the diffusion of the hydrogen.

NOT claim

That is, while an edge portion of a local interconnection in Figs. 17, 19, 20, 21 and 23 of **Mochizuki** maybe arranged above an edge portion of one side of a capacitor, however, in a plan view, as shown Fig. 8, since the local interconnection 22 is formed inside the upper electrode 19, clearly, the local interconnection 22 does not cover an entire portion of the upper electrode 19 with an area which is larger than an area where the upper electrode contacts with the oxide dielectric film in a plan view.

Accordingly, since hydrogen is the smallest element, the hydrogen is diffused to the capacitor via a second insulating film from an edge portion of the local interconnection. That is, diffusion to the capacitor of hydrogen used in the step of forming the third insulating film on the local interconnection can not be prevented in **Mochizuki** completely since, as shown in the plan view of Fig. 8 of **Mochizuki**, local interconnection 22 does not cover an entire portion of the upper electrode 19

In other words, in amended claims 1 and 21, since the local interconnection is formed with covering and an entire portion of the upper electrode with an area which is larger than an area where the upper electrode contacts with the oxide dielectric film in a plan view, diffusion of hydrogen to the capacitor can be completely prevented.

Additionally, the Examiner takes the position that it is described in **Mochizuki** that the local interconnection is a blocking layer for preventing the diffusion of hydrogen without indicating which

portion of **Mochizuki** such description can be found. Accordingly, it is respectfully requested that the Examiner provide specific column and line portions of **Mochizuki** which support the Examiner's position outlined above.

In new claim 22, a local interconnection is formed with surrounding and protruding portion having a fixed size from all edges of an area where the upper electrode contact with the oxide dielectric film. As a result, even if there is an influence of diffusion of hydrogen to the capacitors, the influence is the same between all capacitors, in the result, an action of a circuit including the capacitors is stable.

In contrast, in Fig. 19 of **Mochizuki**, a size covering the capacitor of the local interconnections is different between 36+11' and 22+11', that is, a size covering the capacitor of the local interconnection 36+11" is larger than one of the local interconnection 22+11'. As a result, since the amount of diffusion of hydrogen to the capacitors is different between the two capacitors under the local interconnection 36+11' and 22+11', thus, an action of a circuit including the capacitors is unstable on the basis of the different characterization of the capacitors.

Ochiai does not disclose the step of forming a local interconnection covering an entire portion of the upper electrode with an area which is larger than an area where the upper electrode contact with the oxide dielectric film in a plan view, as recited in amended claims 1 and 21.

That is, an edge of the interconnection 11 is clearly formed inside of the upper electrode 32 in Fig.4 of **Ochiai**.

With regard to **Watanabe**, a step similar to **Ochiai** is disclosed by **Watanabe**. That is, the purpose of **Watanabe** is to prevent peeling between an oxide dielectric film and a lower electrode by diffusion of a reduction gas to a capacitor.

For this reason, a metal nitride film 13, as a cap film, is directly formed on an upper electrode of a capacitor. However, the metal nitride film 13 is directly formed with the same area to the upper electrode of a capacitor.

In contrast, in amended claims 1 and 21, an interconnection is formed with covering an entire portion of the upper electrode with an area which is larger than an area where the upper electrode contact with the oxide dielectric film in a plan view.

Accordingly, the advantage of preventing diffusion of reduction gas into a capacitor is greater in the present claimed invention than in **Watanabe**. Moreover, an interconnection, as shown in Figs.1 to 9 of **Watanabe**, is formed with a smaller area than an area where an upper electrode contacts with an oxide dielectric film.

The applied reference of **Zafer** discloses forming: an impurity diffusion layer 204 in a semiconductor substrate 20; a first insulating film 22 on the semiconductor substrate 20; a lower electrode 242, an oxide dielectric film 244 and an upper electrode 246 as a capacitor; a second insulating film 32 on the capacitor; an opening on the impurity diffusion layer of the upper electrode; an interconnection for connecting the diffusion layer and the upper electrode; and a third insulating firm 524.

The purpose of **Zafer** is to prevent degradation of a polarization-characterization of a dielectric film. For this reason, stress of a second insulating and a third insulating film is controlled so as to make to total the stress of the second insulating and the third insulating film small.

In other words, **Zafer's** purpose is completely different from that of the present claimed invention. Moreover, **Zafer** does not disclose the step of forming a local interconnection covering an entire portion of the upper electrode with an area which is larger than an area where the upper electrode contacts with the oxide dielectric film. That is, an edge of an interconnection, as shown in Figs.4 and 5 of **Zafer**, is clearly formed inside a region where an upper electrode contacts with a dielectric film.

The applied reference of **Kawai** discloses forming: an impurity diffusion layer 26, 26d and a salicie layer 29 in a semiconductor substrate 1; a first insulating film 30; a lower electrode 31, an oxide dielectric film 32 and an upper electrode 33 as a capacitor; a second insulating film 34 on the

capacitor; an opening 36 to 36g on the impurity diffusion layer the upper electrode; an interconnection 37a to 37s for connecting the diffusion layer and the upper electrode; and a third insulation film.

The purpose of **Kawai** is to prevent oxidation of the impurity diffusion layer in the step of annealing with oxygen to recover a deterioration of the oxide dielectric film after the opening of the impurity diffusion layer and the upper electrode. Therefore,the oxidation of the impurity diffusion layer is prevented by the salicide on the impurity diffusion layer.

However, **Kawai** does not disclose forming a local interconnection covering an entire portion of the upper electrode with an area which is larger than an area where the upper electrode contact with the oxide dielectric film in a plan view, as now set forth in amended claims 1 and 21.

That is, the interconnection layer 37a, in Fig.2H of **Kawai**, is formed on an area which is larger than an area where the upper electrode contact with the oxide dielectric film accidentally. Since a plan view of the interconnection and the upper electrode is not disclosed and the purpose of the present claimed invention claim 1 is not described, the interconnection layer 37a, in Fig.2H does not disclose or fairly suggest the features set forth in amended claims 1 and 21.

Thus, for at least these reasons, it is respectfully asserted that the prior art fails to teach or suggest recitations of claims 1-16 and 21 - 22, and request that the Examiner allow these claims,

along with the entire application, to issue. Accordingly, withdrawal of the rejection of claims 1-16 and 21 under 35 U.S.C. §103(a) is respectfully solicited.

Attached hereto is a marked-up version of the changes made tot he claims by the current amendment. The attached page is captioned "**Version with markings to show changes made.**"

If, for any reason, it is felt that this application is not now in condition for allowance, the Examiner is requested to contact Applicants' undersigned attorney at the telephone number indicated below to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed, Applicant respectfully petitions for an appropriate extension of time. The fees for such an extension or any other fees which may be due with respect to this paper, may be charged to Deposit Account No. 01-2340.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

Claims 1, 2, 14 and 21 have been amended as follows:

1. (Twice Amended) A method of manufacturing a semiconductor device comprising the steps

of:

forming an impurity diffusion layer in a semiconductor substrate;

forming a first insulating film covering the semiconductor substrate;

forming a lower electrode of a capacitor on the first insulating film;

forming an oxide dielectric film of the capacitor on the lower electrode;

forming an upper electrode of the capacitor on the oxide dielectric film;

forming a second insulating film for covering the capacitor;

forming a first opening [which exposes] for electrically connecting the impurity diffusion layer and a second opening which exposes the upper electrode in the first and second insulating films, by etching a part of the second insulating film and a part of the first insulating film;

forming a metal film on the second insulating film for connecting electrically the impurity diffusion layer via the first opening and the upper electrode via the second opening;

forming a local interconnection covering an entire portion of the upper electrode with an area which is larger than an area where the upper electrode contacts with the oxide dielectric film in a plain view, in a range which passes through the first opening and the second opening, by patterning the metal film; and

forming a third insulating film for covering the local interconnection.

2. (Twice Amended) A method of manufacturing a semiconductor device according to claim 1, wherein a [an oxidation preventing] metal film constituting the local interconnection is formed of metal nitride.

14. (Twice Amended) A method of manufacturing a semiconductor device according to claim 1 further comprising the step of:

forming a conductive plug between the [oxidation-preventing] metal film and the impurity diffusion layer in the first opening.

21. (Twice Amended) A method of manufacturing a semiconductor device comprising the steps of :

forming an impurity diffusion layer in a semiconductor substrate;

forming a first insulating film covering the semiconductor substrate;

forming a lower electrode of a capacitor on the first insulating film;

forming an oxide dielectric film of the capacitor on the lower electrode;

forming an upper electrode of the capacitor on the oxide dielectric film;

forming a second insulating film for covering the capacitor;

forming a first opening [which exposes] for electrically connecting the impurity diffusion layer and a second opening which exposes the upper electrode in the first and second insulating films, by etching a part of the second insulating film and a part of the first insulating film;

forming a metal film on the second insulating film for connecting electrically the impurity diffusion layer via the first opening and the upper electrode via the second opening;

forming a local interconnection covering an entire portion of the upper electrode with an area which is larger than an area where the upper electrode contacts with the oxide dielectric film in a plan view, in a range which passes through the first opening and the second opening, by patterning the metal film, wherein the local interconnection is a blocking layer for preventing a diffusion of a redundant to the oxide dielectric film; and

forming a third insulating film for covering the local interconnection.